CLAIMS

1.   A method comprising steps of:

receiving a plurality of parameter values for a multi-component circuit having at

least one subcircuit model, said plurality of parameter values determining a plurality of

5   parasitic values of said multi-component circuit;

generating a layout of said multi-component circuit utilizing said plurality of

parameter values, said layout causing said multi-component circuit to have said plurality

of parasitic values.

2.   The method of claim 1 further comprising a step of utilizing said plurality

of parasitic values to simulate an electrical behavior of said multi-component circuit prior

to said generating step.

3.   The method of claim 1 wherein said plurality of parameter values comprise

15   a style parameter value.

4.   The method of claim 1 wherein said plurality of parameter values

comprises a bulk contact parameter value.

20   5.   The method of claim 1 wherein each of said plurality of parameter values is

selected from the group consisting of finger width, finger length, number of fingers,

current, style, slice, and bulk contact parameter values.

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6. The method of claim 1 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of parasitic capacitor values.

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7. The method of claim 6 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

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8. The method of claim 6 further comprising a step of utilizing said plurality of resistor values and said plurality of capacitor values to simulate an electrical behavior of said multi-component circuit prior to said generating step.

9. The method of claim 3 wherein said style parameter value determines how

15 interconnect lines are routed in said layout of said multi-component circuit.

10. The method of claim 4 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said multi-component circuit.

20 11. A method for designing a circuit block including at least one multi-component circuit, said multi-component circuit having at least one subcircuit model, said method comprising steps of:

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receiving a plurality of parameter values for said at least one multi-component

circuit;

determining a plurality of parasitic values for said at least one multi-component

circuit;

5   simulating an electrical behavior of said circuit block utilizing said plurality of

parasitic values;

generating a layout of said circuit block including said at least one multi-

component circuit, said layout causing said at least one multi-component circuit to have

said plurality of parasitic values.

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12.   The method of claim 11 further comprising a step of performing a design

rule check after said step of generating said layout.

13.   The method of claim 11 further comprising a step of performing a layout

15   versus schematic verification after said step of generating said layout.

14.   The method of claim 11 further comprising a step of extracting interconnect

parasitics after said step of generating said layout.

20   15.   The method of claim 11 wherein said plurality of parameter values

comprise a style parameter value.

16.   The method of claim 11 wherein said plurality of parameter values comprises a bulk contact parameter value.

17.   The method of claim 11 wherein each of said plurality of parameter values

5   is selected from the group consisting of finger width, finger length, number of fingers, current, style, slice, and bulk contact parameter values.

18.   The method of claim 11 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of

10   parasitic capacitor values.

19.   The method of claim 18 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

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20.   The method of claim 18 further comprising a step of utilizing said plurality of resistor values and said plurality of capacitor values to simulate an electrical behavior of said at least one multi-component circuit prior to said step of generating said layout.

20   21.   The method of claim 15 wherein said style parameter value determines how interconnect lines are routed in said layout of said at least one multi-component circuit.

22. The method of claim 16 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said at least one multi-component circuit.

5   23. A system comprising a computer for designing a circuit block including at least one multi-component circuit, said at least one multi-component circuit having at least one subcircuit model, said computer implementing a method comprising steps of:

said computer receiving a plurality of parameter values for said at least one multi-component circuit in said circuit;

10   said computer determining a plurality of parasitic for said at least one multi-component circuit;

said computer generating a layout of said at least one multi-component circuit utilizing said plurality of parameter values, said layout causing said at least one multi-component circuit to have said plurality of parasitic values.

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24. The system of claim 23 wherein said method further comprises a step of said computer utilizing said plurality of parasitic values to simulate an electrical behavior of said at least one multi-component circuit prior to said step of said computer generating said layout.

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25. The system of claim 23 wherein said method further comprises a step of said computer performing a design rule check after said step of said computer generating said layout.

5 26. The system of claim 23 wherein said method further comprises a step of said computer performing a layout versus schematic verification after said step of said computer generating said layout.

10 27. The system of claim 23 wherein said method further comprises a step of said computer extracting interconnect parasitics after said step of said computer generating said layout.

28. The system of claim 23 wherein said plurality of parameter values comprise a style parameter value.

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29. The system of claim 23 wherein said plurality of parameter values comprises a bulk contact parameter value.

30. The system of claim 23 wherein each of said plurality of parameter values

20 is selected from the group consisting of finger width, finger length, number of fingers, current, style, slice, and bulk contact parameter values.

31. The system of claim 23 wherein said parasitic values of said at least one subcircuit model comprise a plurality of parasitic resistor values and a plurality of parasitic capacitor values.

5   32. The system of claim 31 wherein said plurality of parasitic resistor values and said plurality of parasitic capacitor values are determined by said plurality of parameter values.

33. The system of claim 28 wherein said style parameter value determines how 10 interconnect lines are routed in said layout of said at least one multi-component circuit.

34. The system of claim 29 wherein said bulk contact parameter value determines a location for bulk contacts in said layout of said at least one multi-component circuit.